

Makefile

Quick reference https://www.gnu.org/software/make/manual/html_node/Quick-Reference.html

[Recursive Make Considered Harmful](#)

<http://make.mad-scientist.net/papers/rules-of-makefiles/>

one shell

5.3.1 Using One Shell

```
.ONESHELL:
foo : bar/lose
    cd $(<D)
    gobble $(<F) > ../$@
```

disable built-in rules

```
# Disable built-in rules and variables
MAKEFLAGS += --no-builtin-rules
MAKEFLAGS += --no-builtin-variables
```

VPATH

https://www.gnu.org/software/make/manual/html_node/General-Search.html

VPATH tells makefile where to search for prerequisites:

```
VPATH = .:$(OBJDIR):$(LIBDIR)
```

order only prereq

Special pipe “|” character is used. If any *\$(objects)* has to be build, then *obj* has to be build first. But if *obj* is out of date or missing, this doesn't force *\$(objects)* to build.

```
$(objects): | obj
obj:
    @mkdir -p $@'
```

```
targets : normal-prerequisites | order-only-prerequisites
```

https://www.gnu.org/software/make/manual/html_node/Prerequisite-Types.html

double colon rules

https://www.chemie.fu-berlin.de/chemnet/use/info/make/make_4.html#SEC40

It can be useful, when target needs to be updated and command to update target depends on which prerequisite file caused the update.

```
all::
```

Another scenario is to find source .c file in different dirs

```
build/%.o:: test/%.c
    $(COMPILE) $(CFLAGS) $< -o $@

build/%.o:: src/%.c
    $(COMPILE) $(CFLAGS) $< -o $@

build/%.o:: lib/src/%.c lib/src/%.h
    $(COMPILE) $(CFLAGS) $< -o $@
```

- The same target can appear in more than one rule
- each rule is executed if target is older than any prerequisite of that rule
 - if no prereq, command is always executed
- Order of execution is not guaranteed

Parallel make

Disabling parallel

For whole file:

```
.NOTPARALLEL:
```

For single target:

```
.NOTPARALLEL: %.a
.NOTPARALLEL: foo.c bar.c
```

[Parallel makefile requires dependency ordering](#)

Prevent one target from parallel run

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