

Overclocking

```
insmod /lib/modules/cpu_frequ.ko
cat /proc/cpu_frequ/pll0_ndiv_mdiv
Modul HZ = 1000
CKGA_LCK = 0
CKGA_MD_STA = 6
CKGA_PLL0_CFG = 83b06
CKGA_PLL0_LCK_STA = 1
CKGA_PLL0_CLK1 = 0
CKGA_PLL0_CLK2 = 1
CKGA_PLL0_CLK3 = 0
CKGA_PLL0_CLK4 = 0
CKGA_PLL1_CFG = 98009
CKGA_PLL1_LCK_STA = 1
CKGA_CLK_DIV = 0
CKGA_CLK_EN = 3f
CKGA_PLL1_BYPASS = 0
CKGA_CLKOUT_SEL = 0
SYSCLKOUT (standard 266MHz) = 265MHz
TMU0_TCOR = 10347
TMU0_TCNT = 7621
TMU1_TCOR = ffffffff
TMU1_TCNT = 334689d3
```

```
BOGOMIPS (static)= 262
BOGOMIPS (measured)= 261
```

```
PLL0      = 531 MHz
SH4       = 265 MHz
SH4_IC    = 132 MHz
MODULE    = 66 MHz
SLIM      = 265 MHz
PLL1      = 384 MHz
COMMS     = 96 MHz
TMU0      = 16 MHz
TMU1      = 16 MHz
```

```
sh4 ratio (2,4,6,8,12,16)
sh4_ic ratio (2,4,6,8,12,16)
module ratio (4,8,12,16)
slim ratio (2,4,6,8,12,16)
```

```
int ndiv_mdiv=simple_strtoul(buffer, NULL, 10);
#ifdef STB7100
    mdiv = (ndiv_mdiv >> 0) & 0xff;
    ndiv = (ndiv_mdiv >> 8) & 0xff;

    regdata = ctrl_inl(CKGA_PLL1_CFG); // get data from register
    regdata = regdata | mdiv; // set MDIV
```

```
regdata = regdata | ndiv << 8; // set NDIV
regdata = regdata | (0x1 & 0x7) << 16; // set PDIV
ctrl_outl(regdata, CKGA_PLL1_CFG);
```

CKGA_PLL0_CFG = 83b06 = 539398

Wg: <http://forum.xunil.pl/index.php/topic,3128.msg42823.html#msg42823>

Ogólnie wpisuje się do rejestru [/proc/cpu_frequ/pll0_ndiv_mdiv] ($N \cdot 256 + M$) i wzór jest taki na PLL0:

$$\text{PLL0_CLK} = \text{EXT_CLOCK} * 2 * N / M$$

EXT_CLK w moim ESI (7105) to 30MHz a w nboksie (7100) 27MHz. Domyślnie w ESI mam $N=15$, $M=1$.

Zakresy M i N są ograniczone.

dla 7105/7111: M od 0 do 7 i N od 3 do 255
dla 7100: M od 0 do 255 i N od 3 do 255

Nie wiem co będzie jak się ustawi $M=0$;)

Teoretycznie najniższa częstotliwość dla 7105 to ok. 12,8MHz po wpisaniu do /proc/cpu_frequ/pll0_ndiv_mdiv wartości $3 \cdot 256 + 7$.

echo 5377 > /proc/cpu_frequ/pll0_ndiv_mdiv # hangs

366MHz echo 31241 > /proc/cpu_frequ/pll0_ndiv_mdiv

3841 = 450mhz 12803 = 500mhz 5121 = 600mhz 16643 = 650mhz 17923 = 700mhz

als beispiel für 650mhz: echo 16643 > /proc/cpu_frequ/pll0_ndiv_mdiv

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