Cortex-M

Cortex-M doesn't support ARM instruction set. It only supports "Thumb" instruction set. Bit 0 from PC is copied to T bit in xPSR. It instructs CPU about next instruction mode (0-ARM mode, 1-thumb mode). If T bit is zero, `Usage fault` exception is raised.

Compiler puts odd address into register which is next used to branch. During branch value from branch argument is copied to PC (without bit zero) so PC value is even and bit 0 is copied into xPSR T bit.

hardfault with PC: 0xfffffffd

LR = 0xFFFFFFFD means that the return stack is the PSP (not the MSP).

hardfault with PC: 0xfffffffe

Cortex M has only 31:1 bits in PC register (even addresses only). This address is a special LOCKUP address. It means CPU cannot continue. Probably during handling fault another fault occurs.

hardfault with PC: 0xfffffe9

- 8.7 EXC_RETURN
- Exception Return